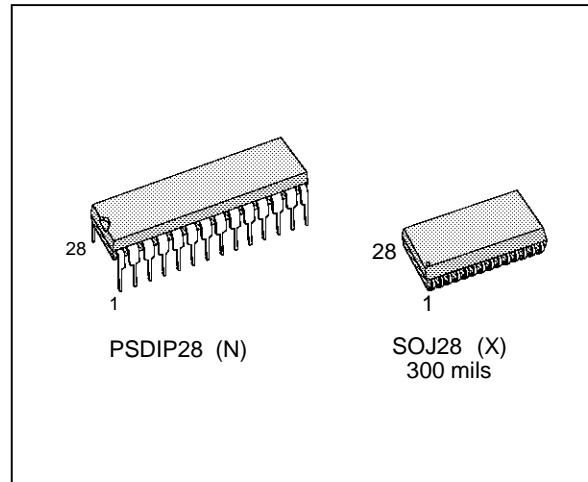


VERY FAST CMOS 8K x 8 CACHE TAGRAM

- 8K x 8 CMOS SRAM with ON BOARD COMPARATOR
- ADDRESS to COMPARE ACCESS TIME: 15, 17, 20, 25ns
- FAST CHIP SELECT COMPARE ACCESS: 8ns
- MATCH OUTPUT with FAST TAG DATA to COMPARE ACCESS of: 12, 15ns Max
- STATIC OPERATION-NO CLOCKS or TIMING STROBES REQUIRED
- FULL CMOS for LOW POWER OPERATION.
- TOTEM-POLE MATCH OUTPUT
- THREE-STATE OUTPUTS
- 28 PIN 300 MIL DIP & 28 PIN 300 MIL SOJ
- HIGH SPEED ASYNCHRONOUS RAM CLEAR



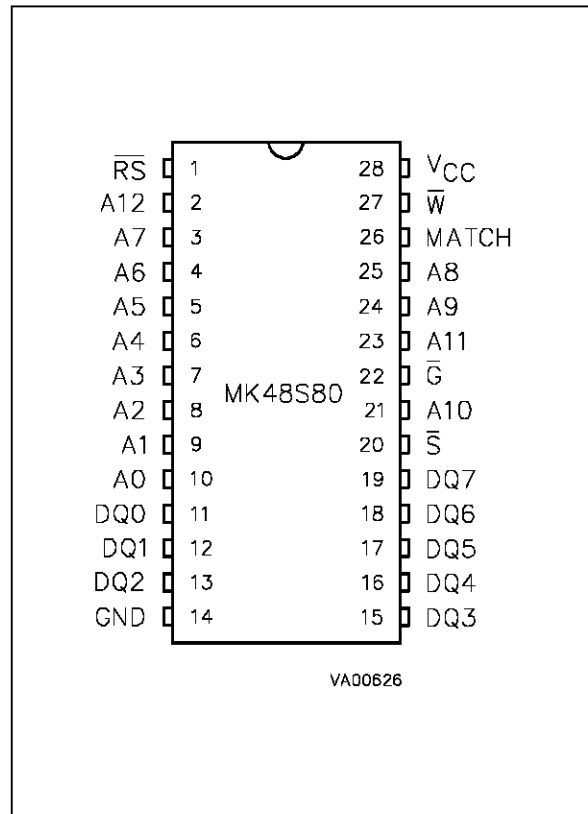
TRUTH TABLE

| \overline{W} | \overline{S} | \overline{G} | \overline{RS} | Mode | DQ | Match |
|----------------|----------------|----------------|-----------------|-------------|------------------|-------|
| X | X | X | L | Reset Clear | High-Z | High |
| X | H | X | H | Deselect | High-Z | High |
| H | L | H | H | Miss | D _{IN} | Low |
| H | L | H | H | Match | D _{IN} | High |
| H | L | L | H | Read | Q _{OUT} | High |
| L | L | X | H | Write | D _{IN} | High |

PIN NAMES

| | |
|-----------------------|-----------------------|
| A0 - A12 | Address Inputs |
| DQ0 - DQ7 | Data Inputs / Outputs |
| MATCH | Comparator Output |
| \overline{S} | Chip Select |
| \overline{G} | Output Enable |
| \overline{W} | Write Enable |
| \overline{RS} | Reset Flash Clear |
| V _{CC} , GND | 5 Volts, Ground |

Figure 1. Pin Connection



MK48S80

DESCRIPTION

The MK48S80 is a 65,536 fast static cache TAGRAM™ organized as 8K x 8 bits. It is fabricated using SGS-THOMSON's low power, high performance HCMOS4 technology. The MK48S80 features fully static operation requiring no external clocks or timing strobes. The device requires a single 5V supply and is fully TLL compatible. The MK48S80 has a fast Chip Select control for high speed operation to the Match Compare valid, and device select/deselect operations. Additionally, the MK48S80 provides a Reset Clear, and MATCH compare pin. The Reset Clear input provides an asynchronous RAM clear control which clears all internal RAM bits to zero. The MATCH output is in a totem-pole configuration to minimize switching delays associated with open-drain devices. During a MATCH compare cycle, an on-board 8-bit comparator compares the Data Inputs (8-bit TAG) at the specified address index (A0-A12) to the internal RAM data. If a miss condition exists, where at least one bit of TAG data does not match the internal RAM, then the MATCH output issues a LOW miss signal.

OPERATIONS

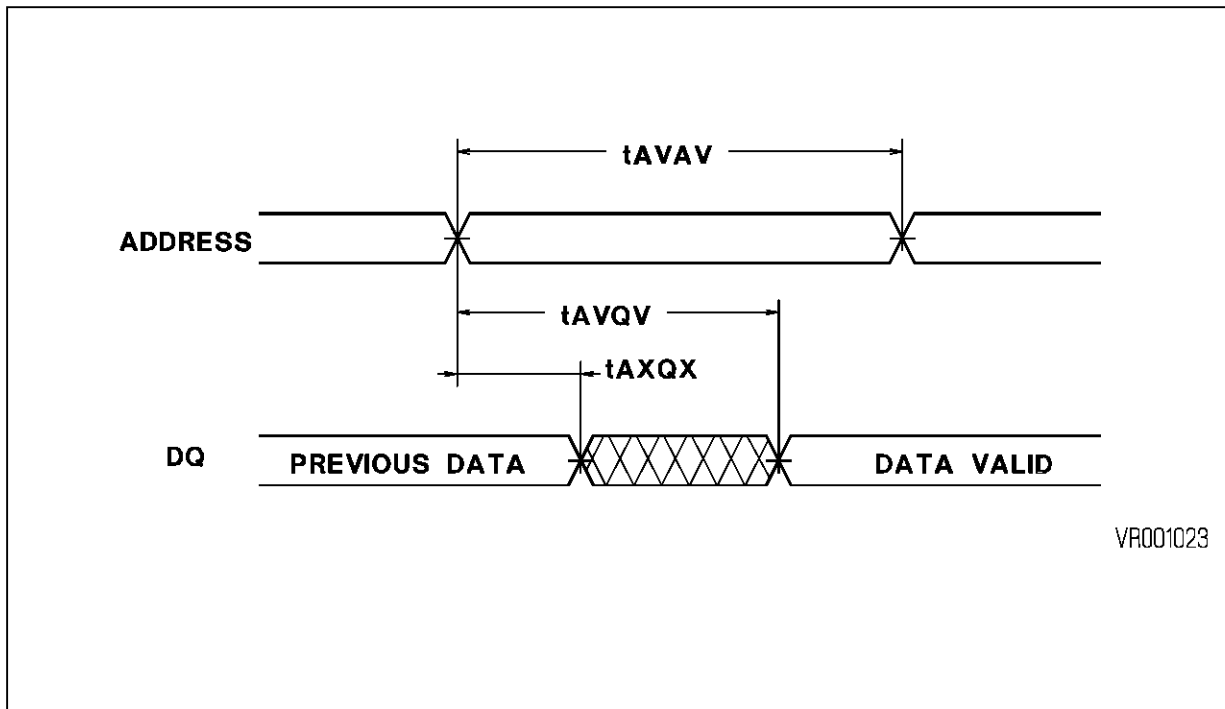
READ MODE

The MK48S80 is in the read mode whenever Write Enable (\bar{W}) is HIGH with Output Enable (\bar{G}) LOW, and Chip Select (\bar{S}) is active. This provides access to data from eight of 65,536 locations in the static memory array. The unique address specified by the 13 Address Inputs defines which one of the 8192 8-bit bytes is to be accessed. Valid data will be available at the eight Output pins within t_{AVQV} after the last stable address, providing \bar{G} is LOW, and \bar{S} is LOW. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{SLQV} or t_{GLQV}) rather than the addresses. The state of the DQ pins is controlled by the \bar{S} , \bar{G} , and \bar{W} control signals. Data out may be indeterminate at t_{SLQX} and t_{GLQX} , but data line will always be valid at t_{AVQV} .

READ CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions (0 °C ≤ T_A ≤ +70 °C; V_{CC} = 5V ± 5%)

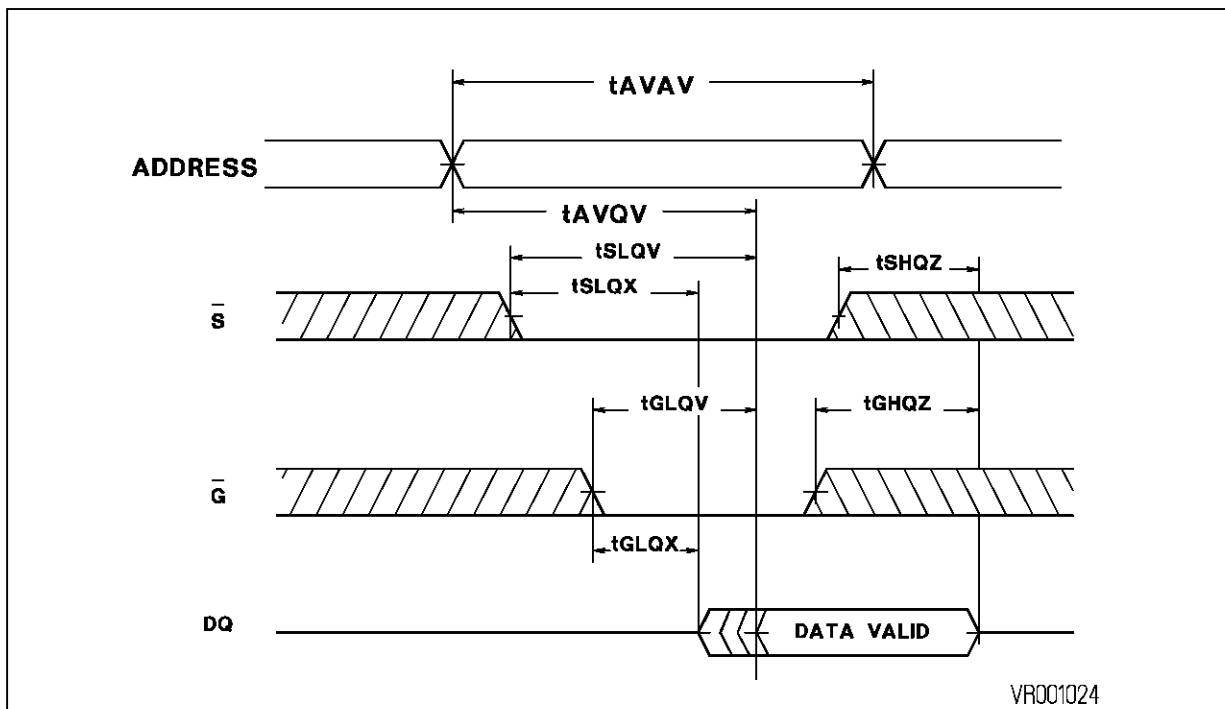
| Symbol | | Parameter | 15 | | 17 | | 20 | | 25 | | Unit | Note |
|-------------------|------------------|---------------------------------|------|------|------|------|------|------|------|------|------|------|
| Std | Alt | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| t _{AVAV} | t _{RC} | Read Cycle Time | 20 | | 20 | | 20 | | 25 | | ns | |
| t _{AVQV} | t _{AA} | Address Access Time | | 20 | | 20 | | 20 | | 25 | ns | 1 |
| t _{SLQV} | t _{CSA} | Chip Select Access Time | | 15 | | 15 | | 15 | | 15 | ns | |
| t _{GLQV} | t _{OEA} | Output Enable Access Time | | 10 | | 10 | | 10 | | 15 | ns | 1 |
| t _{SLQX} | t _{CSL} | Chip Select to Output Low-Z | 0 | | 0 | | 0 | | 0 | | ns | |
| t _{GLQX} | t _{OEL} | Output Enable to Low-Z | 0 | | 0 | | 0 | | 0 | | ns | |
| t _{SHQZ} | t _{CSZ} | Chip Select to High-Z | | 9 | | 9 | | 9 | | 9 | ns | |
| t _{GHQZ} | t _{OEZ} | Output Enable to High-Z | | 8 | | 8 | | 8 | | 8 | ns | 2 |
| t _{AXQX} | t _{OH} | Output Hold From Address Change | 3 | | 3 | | 3 | | 3 | | ns | 1 |

Figure 2. Read Timing No. 1 (Address Access)



Note: Chip Select and Output Enable are presumed Valid, $W = V_{IH}$

Figure 3. Read Timing No. 2 ($W = V_{IH}$)



WRITE MODE

The MK48S80 is in the Write mode whenever the \overline{W} and \overline{S} pins are LOW. Chip Select or \overline{W} must be inactive during Address transitions. The Write begins with the concurrence of Chip Select being active with \overline{W} LOW. Therefore address setup times are referenced to Write Enable and Chip Select as t_{AVWL} and t_{AVSL} , and is determined to the latter occurring edge. The Write cycle can be terminated

by the earlier rising edge of \overline{S} or \overline{W} . If the output is enabled ($\overline{S} = \text{LOW}$, $\overline{G} = \text{LOW}$), then \overline{W} will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of Write Enable, or to the rising edge of \overline{S} , whichever occurs first, and remain valid t_{WHDX} after the rising edge of \overline{S} or \overline{W} .

WRITE CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions
 (0 °C ≤ T_A ≤ +70 °C; V_{CC} = 5V ± 5%)

| Symbol | | Parameter | 15 | | 17 | | 20 | | 25 | | Unit | Note |
|-------------------|------------------|--------------------------------------|------|------|------|------|------|------|------|------|------|------|
| Std | Alt | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| t _{AVAV} | t _{WC} | Write Cycle Time | 20 | | 20 | | 20 | | 25 | | ns | |
| t _{AVWL} | t _{AS} | Address Set-up to Write Enable Low | 0 | | 0 | | 0 | | 0 | | ns | |
| t _{AVSL} | t _{AS} | Address Set-up to Chip Select | 0 | | 0 | | 0 | | 0 | | ns | |
| t _{AVWH} | t _{AW} | Address Valid to End of Write | 15 | | 15 | | 15 | | 20 | | ns | |
| t _{WLWH} | t _{WEW} | Write Pulse Width | 15 | | 15 | | 15 | | 20 | | ns | |
| t _{WHAX} | t _{AH} | Address Hold Time After End of Write | 0 | | 0 | | 0 | | 0 | | ns | |
| t _{SLSH} | t _{CSW} | Chip Select to End of Write | 15 | | 15 | | 15 | | 20 | | ns | |
| t _{SHAX} | t _{WR} | Write Recovery Time to Chip Select | 0 | | 0 | | 0 | | 0 | | ns | |
| t _{DVWH} | t _{DW} | Data Valid to End of Write | 10 | | 10 | | 10 | | 13 | | ns | |
| t _{WHDX} | t _{DH} | Data Hold Time | 0 | | 0 | | 0 | | 0 | | ns | |
| t _{WHQX} | t _{WEL} | Write High to Output Low-Z (Active) | 0 | | 0 | | 0 | | 0 | | ns | 2 |
| t _{WLQZ} | t _{WEZ} | Write Enable to Output High-Z | | 5 | | 5 | | 5 | | 5 | ns | 2 |

Figure 4. Writing Timing No. 1 (Write Control)

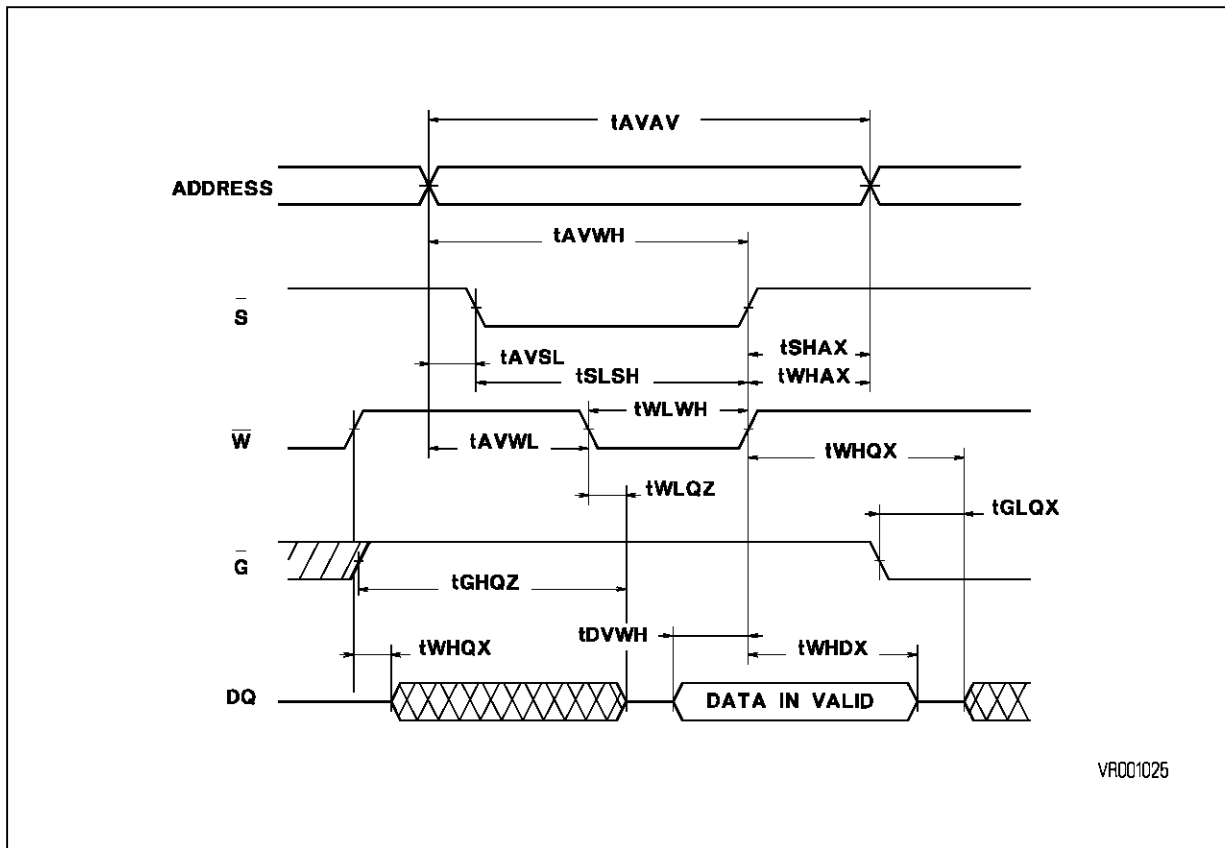
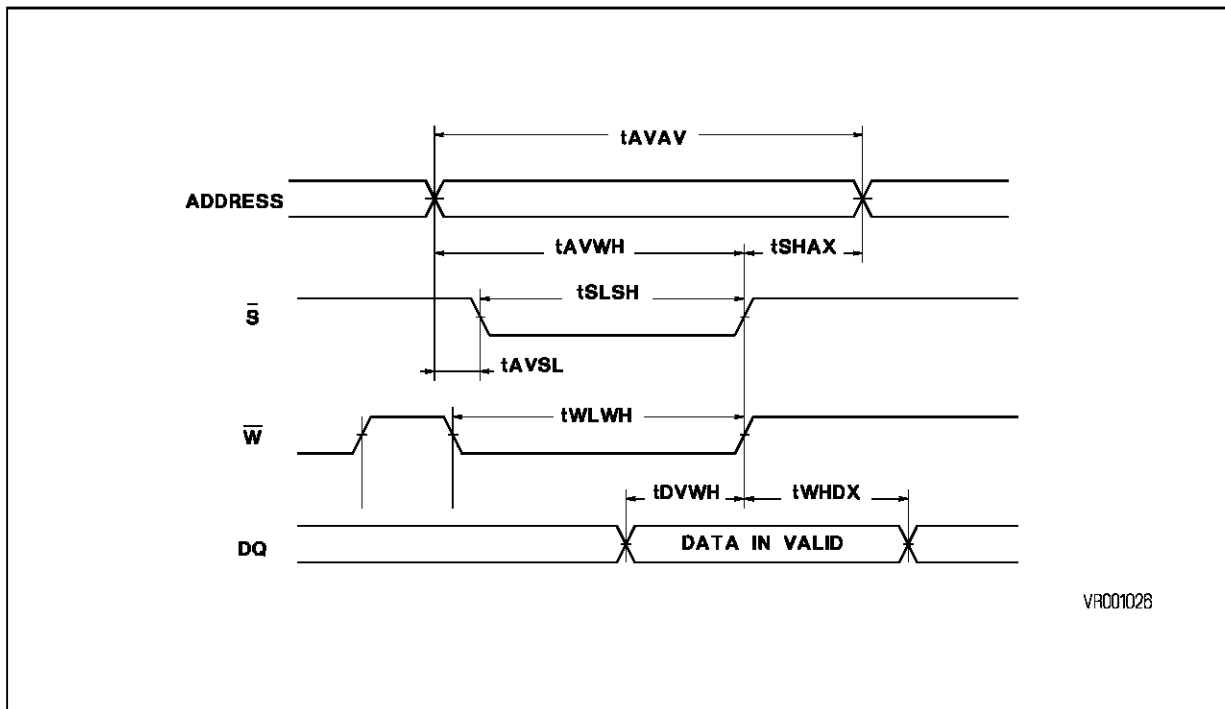


Figure 5. Writing Timing No. 2 (Chip Select Control)



Note: $\bar{G} = V_{IH}$

COMPARE MODE

The MK48S80 is in the Compare mode whenever \overline{W} and \overline{G} are HIGH provided Chip Select (\overline{S}) is active LOW. The 13 index address inputs (A0-A12) define a unique location in the static RAM array. The data presented on the Data Inputs (DQ0-DQ7) as Tag Data is compared to the internal RAM data as specified by the index. If all bits are equal, then a hit condition occurs (MATCH = HIGH). When at least one bit is not equal, then MATCH will go LOW signifying a miss condition. The MATCH output will be valid t_{AVMV} from stable address, or t_{VMV} from valid Tag Data when S is LOW. Should the address be stable with valid Tag Data, and the device is deselected ($\overline{S} = \text{HIGH}$), then MATCH will be valid t_{SLMV} from the falling edge of Chip Select (\overline{S}). When executing a write-to-compare cycle ($\overline{W} = \text{LOW}$, $\overline{G} = \text{LOW}$ or HIGH), MATCH will be valid t_{WHMV} or t_{GHMV} from the latter rising edge of \overline{W} or \overline{G} respectively.

RESET MODE

The MK48S80 allows an asynchronous reset clear whenever \overline{RS} is LOW regardless of the logic state on the other input pins. Reset clears all internal RAM bits (65,536 bits) to a logic zero as long as $t_{RSL-RSH}$ is satisfied. The state of the outputs is

determined by the control logic input pins \overline{S} , \overline{W} , and \overline{G} during reset (see Truth Table). The MATCH output will go HIGH t_{RSL-MH} from the falling edge of \overline{RS} , and all inputs will not be recognized until t_{RSH-AV} from the rising edge of reset (\overline{RS}).

APPLICATION

The MK48S80 operates from a 5V supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. A pull-up resistor is also recommended for the \overline{RS} input. This will ensure that any low going system noise, coupled onto the input does not drive \overline{RS} below V_{IH} minimum specifications. This will enhance proper device operation, and avoid possible partial flash clear cycles. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the MK48S80 can also interface to 5V CMOS on all inputs and outputs. The MK48S80 provides the system designer with 64K fast static memory, a MATCH output-pin, and a BYTEWIDE on-board comparator, all in one chip. The MK48S80 compares the contents of addressed RAM locations to the current data inputs. A logic one "1" output on the MATCH pin indicates that the input data and the RAM data

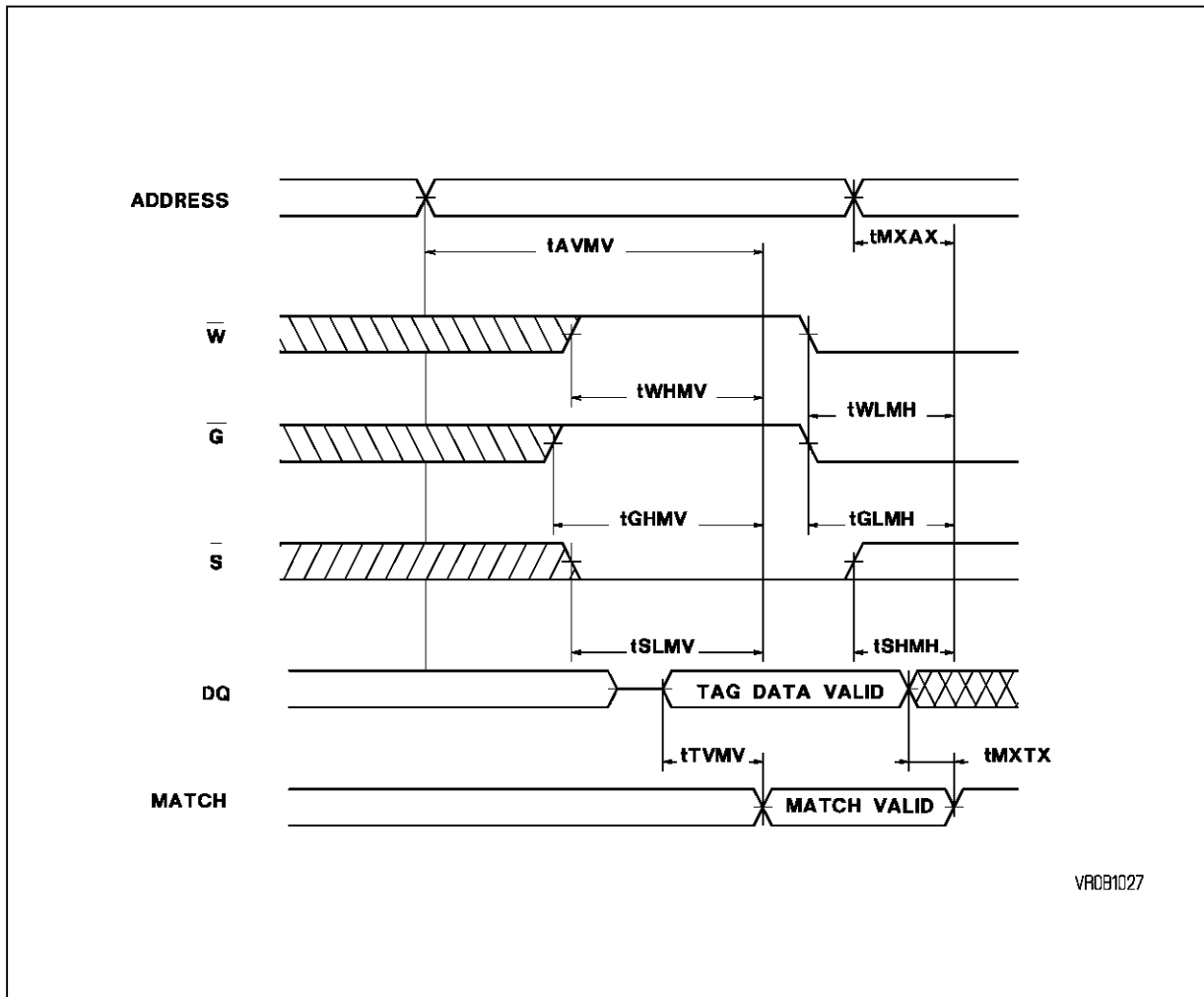
COMPARE CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions
(0 °C ≤ T_A ≤ +70 °C; V_{CC} = 5V ± 5%)

| Symbol | | Parameter | 15 | | 17 | | 20 | | 25 | | Unit | Note |
|------------|------------|------------------------------------|------|------|------|------|------|------|------|------|------|------|
| Std | Alt | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| t_{AVMV} | t_{AMA} | Address to MATCH Valid | | 15 | | 17 | | 20 | | 25 | ns | 1 |
| t_{SLMV} | t_{CSM} | Chip Select to MATCH Valid | | 8 | | 8 | | 10 | | 15 | ns | 1 |
| t_{SHMH} | t_{CSMH} | Chip Deselect to MATCH High | | 5 | | 5 | | 8 | | 12 | ns | 1 |
| t_{VMV} | t_{DMA} | Tag Data to MATCH Valid | | 12 | | 12 | | 12 | | 15 | ns | 1 |
| t_{GHMV} | t_{OEM} | \overline{G} High to MATCH Valid | | 10 | | 10 | | 10 | | 15 | ns | 1 |
| t_{GLMH} | t_{OEMH} | \overline{G} Low to MATCH High | | 10 | | 10 | | 10 | | 12 | ns | 1 |
| t_{WHMV} | t_{WEM} | \overline{W} High to MATCH Valid | | 10 | | 10 | | 10 | | 20 | ns | 1 |
| t_{WLMH} | t_{WEMH} | \overline{W} Low to MATCH High | | 10 | | 10 | | 10 | | 15 | ns | 1 |
| t_{MXAX} | t_{MHA} | MATCH Hold From Address | 1 | | 1 | | 1 | | 1 | | ns | 1 |
| t_{MXTX} | t_{MHD} | MATCH Hold From Tag Data | 0 | | 0 | | 0 | | 0 | | ns | 1 |

RESET CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions
 (0 °C ≤ T_A ≤ +70 °C; V_{CC} = 5V ± 5%)

| Symbol | | Parameter | 15 | | 17 | | 20 | | 25 | | Unit |
|----------------------|------------------|--|------|------|------|------|------|------|------|------|------|
| Std | Alt | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{RSC} | t _{RC} | Flash Clear Cycle Time | 80 | | 80 | | 80 | | 80 | | ns |
| t _{RSL-AX} | t _{RSX} | Reset Clear (\overline{RS}) to Inputs Don't Care | 0 | | 0 | | 0 | | 0 | | ns |
| t _{RSH-AV} | t _{RSV} | \overline{RS} to Inputs Valid | 5 | | 5 | | 5 | | 5 | | ns |
| t _{RSL-RSH} | t _{RSP} | Reset (\overline{RS}) Pulse Width | 75 | | 75 | | 75 | | 75 | | ns |
| t _{RSL-MH} | t _{RSM} | Reset (\overline{RS}) to MATCH High | | 15 | | 15 | | 15 | | 15 | ns |

Figure 6. Match Compare Timing

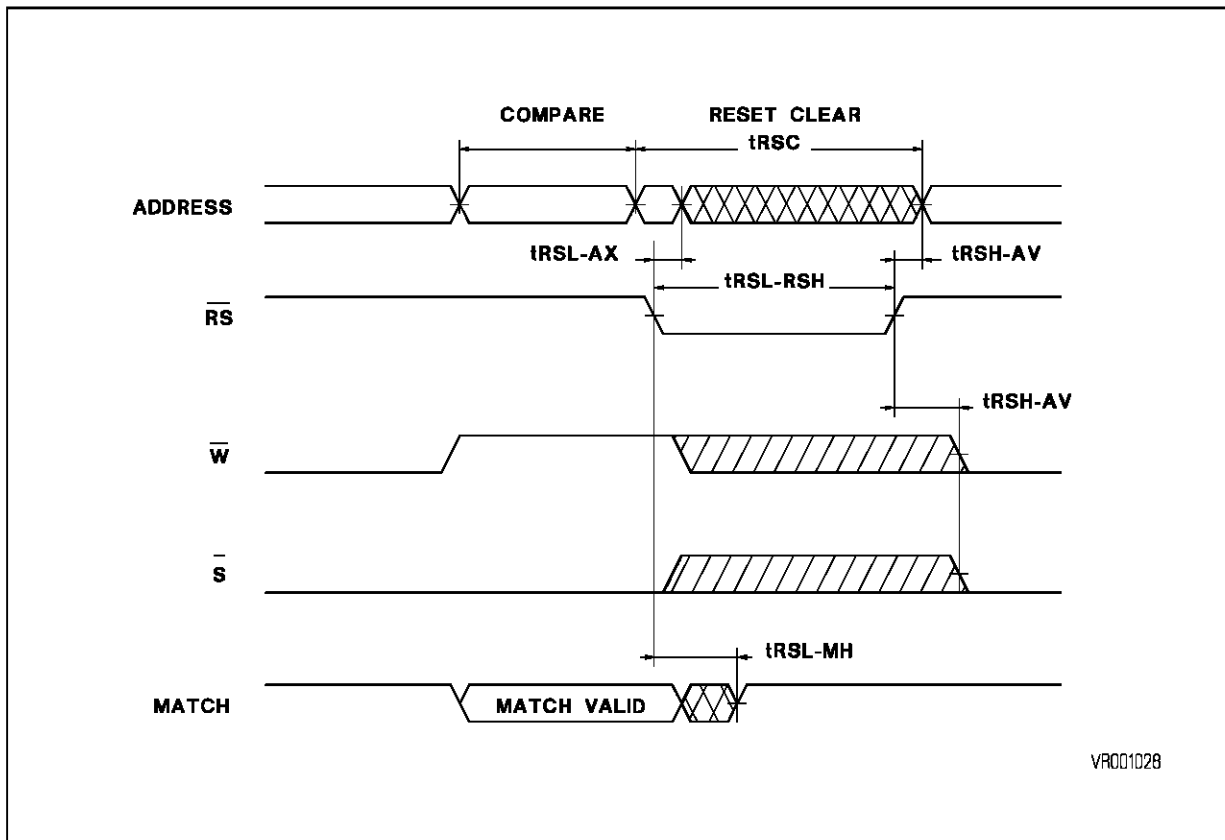


match. Conversely, a logic zero "0" on the MATCH pin indicates at least one bit of difference between the RAM contents and the input TAG, generating a miss.

The MATCH output is constructed with a totem-pole arrangement. The totem-pole configuration allows the designer to minimize switching delays and noise problems associated with open-drain devices. In a cache subsystem, the MATCH signal provides the processor or CPU with the necessary information concerning wait state conditions. The purpose of a cache subsystem is to maintain a duplicate copy of portions of the main memory. When a valid match occurs, the system processor uses data from the fast cache memory, and avoids longer cycles to the main memory. Therefore, implementing cache subsystems with the MK48S80, and providing good hit or match ratio designs will

enhance overall system performance. Because high frequency current transients will be associated with the operation of the MK48S80, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. Though often times not thought of as such, the traces of a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

Figure 7. Reset Timing



Note: \overline{G} = High

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|------------------|---------------------------------------|------------|------|
| V _I | Voltage on any Pin Relative to Ground | -0.3 to 6 | V |
| T _A | Operating Temperature | 0 to 70 | °C |
| T _{STG} | Storage Temperature | -65 to 150 | °C |
| P _D | Power Dissipation | 1 | W |
| I _{OUT} | Output Current | 50 | mA |

Note: This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0 °C ≤ T_A ≤ +70 °C)

| Symbol | Parameter | Min. | Max. | Unit | Notes |
|-----------------|--------------------|------|-----------------------|------|-------|
| V _{CC} | Supply Voltage | 4.75 | 5.25 | V | 3 |
| GND | Ground | 0 | 0 | V | 3 |
| V _{IH} | Logic 1 All Inputs | 2.2 | V _{CC} + 0.3 | V | 3 |
| V _{IL} | Logic 0 All Inputs | -0.3 | 0.8 | V | 3 |

DC ELECTRICAL CHARACTERISTICS (0 °C ≤ T_A ≤ +70 °C; V_{CC} = 5V ± 5%)

| Symbol | Parameter | Min. | Max. | Unit | Notes |
|------------------|---|------|------|------|-------|
| I _{CC1} | Average V _{CC} Power Supply Current | | 160 | mA | 4 |
| I _{IL} | Input Leakage Current | -1 | 1 | μA | 5 |
| I _{OL} | Output Leakage Current | -5 | 5 | μA | 6 |
| V _{OH} | Logic 1 Output Voltage (I _{OUT} = -4 mA) | 2.4 | | μA | 3 |
| V _{OL} | Logic 0 Output Voltage (I _{OUT} = 8 mA) | | 0.4 | V | 3 |

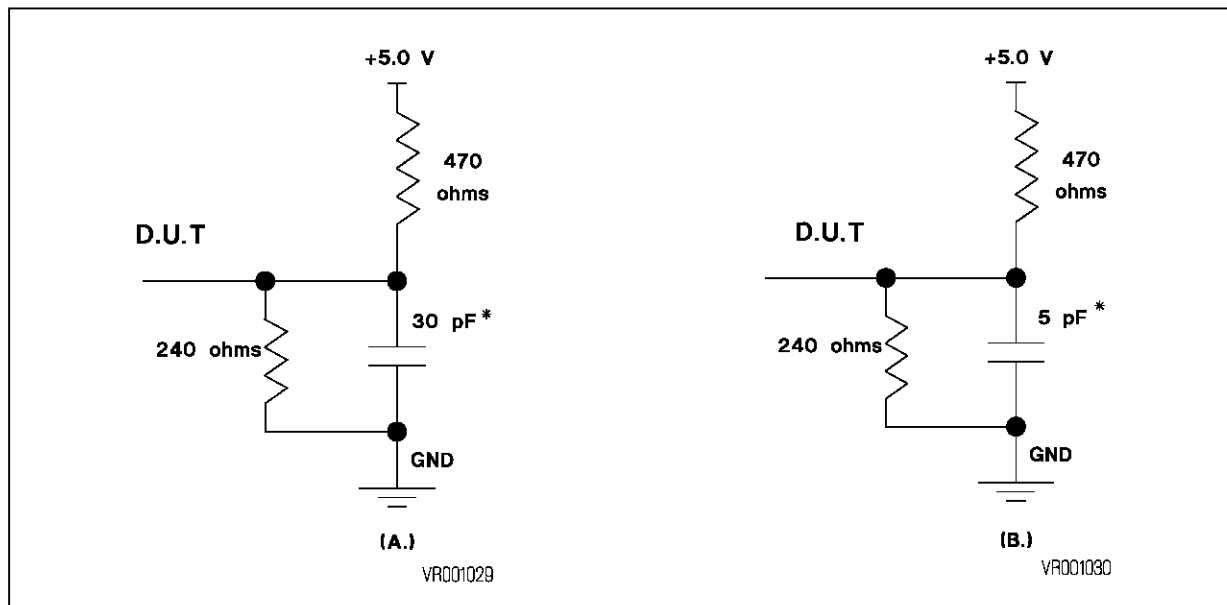
CAPACITANCE (T_A = 25 °C, f = 1MHz)

| Symbol | Parameter | Max. | Unit | Notes |
|------------------|-------------------------------|------|------|-------|
| C _{IN} | Capacitance on all Input pins | 4 | pF | 7 |
| C _{OUT} | Capacitance on Q Output pins | 10 | pF | 7 |

AC TEST CONDITIONS

| Parameter | Value | Unit |
|--|---------|------|
| Input Levels | 0 to 3 | V |
| Transition Time | 1.5 | ns |
| Input and Output Signal Timing Reference Level | 1.5 | V |
| Ambient Temperature | 0 to 70 | °C |
| Supply Voltage | 5 ± 5% | V |

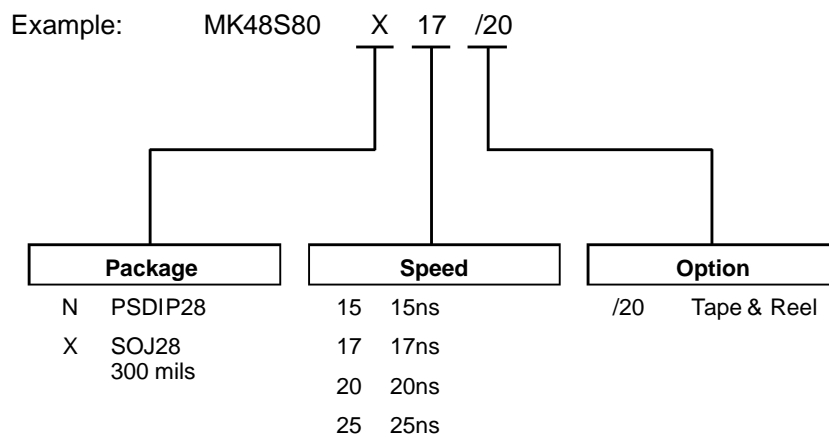
Figure 8. Equivalent Output Load Circuits



Notes :

1. Measured with load shown in Figure 8A.
2. Measured with load shown in Figure 8B.
3. All voltages referenced to GND.
4. I_{CC1} is measured as the average AC current with $V_{CC} = V_{CC}(\text{max})$ and with the outputs open circuit. $t_{AVAV} = t_{AVAV}(\text{min})$ duty cycle 100%.
5. Input leakage current specifications are valid for all V_{IN} such that $0\text{ V} < V_{IN} < V_{CC}$. Measured at $V_{CC} = V_{CC}(\text{max})$.
6. Output leakage current specifications are valid for all V_{OUT} such that $0\text{ V} < V_{OUT} < V_{CC}$, $\bar{S} = V_{IH}$ and V_{CC} in valid operating range.
7. Sampled, not 100% tested.

ORDERING INFORMATION SCHEME

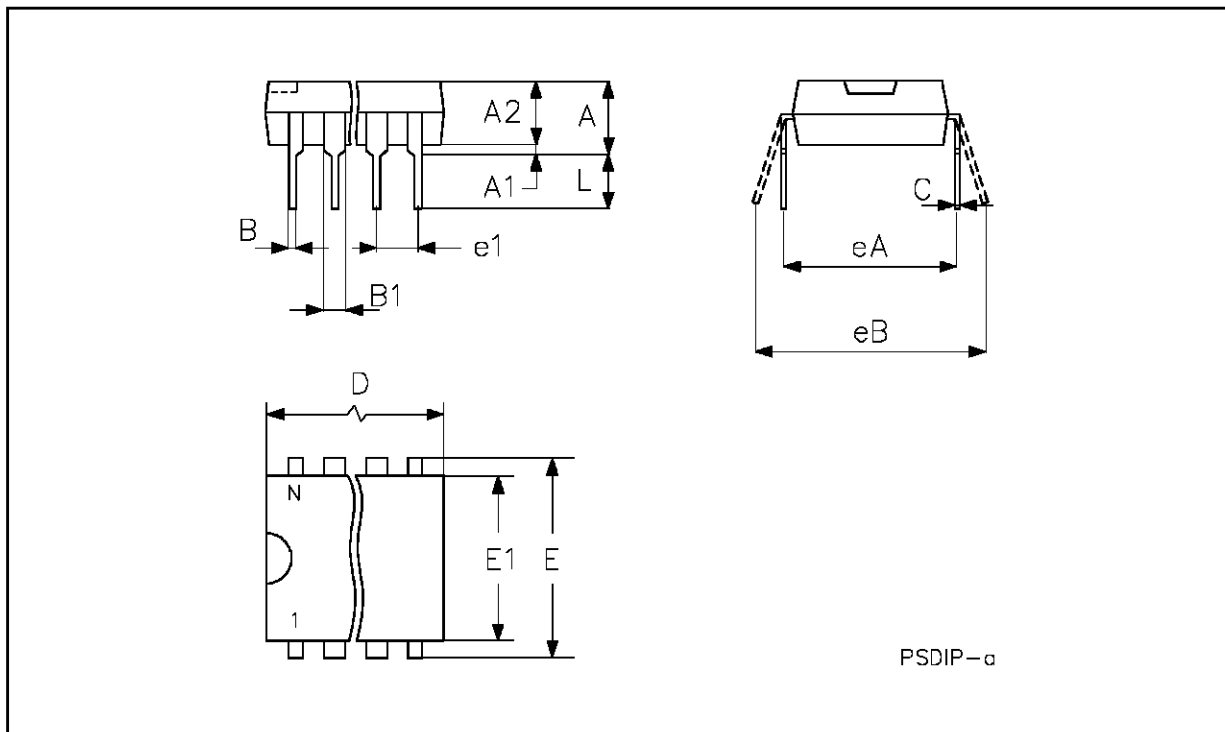


For a list of available options of Package and Speed, refer to the current Memory Shortform catalogue.
 For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP28 - 28 pin Plastic Skinny DIP, 300 mils width

| Symb | mm | | | inches | | |
|------|------|-------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 4.57 | | | 0.180 |
| A1 | | 0.38 | – | | 0.015 | – |
| A2 | | 3.05 | 3.56 | | 0.120 | 0.140 |
| B | | 0.38 | 0.53 | | 0.015 | 0.021 |
| B1 | | 1.14 | 1.27 | | 0.045 | 0.050 |
| C | | 0.20 | 0.30 | | 0.008 | 0.012 |
| D | | 34.54 | 34.80 | | 1.360 | 1.370 |
| E | | 7.62 | 8.26 | | 0.300 | 0.325 |
| E1 | | 7.11 | 7.49 | | 0.280 | 0.295 |
| e1 | 2.54 | – | – | 0.100 | – | – |
| eA | 7.62 | – | – | 0.300 | – | – |
| eB | | | 10.92 | | | 0.430 |
| L | | 3.18 | 3.43 | | 0.125 | 0.135 |
| N | | 28 | | | 28 | |

PSDIP28



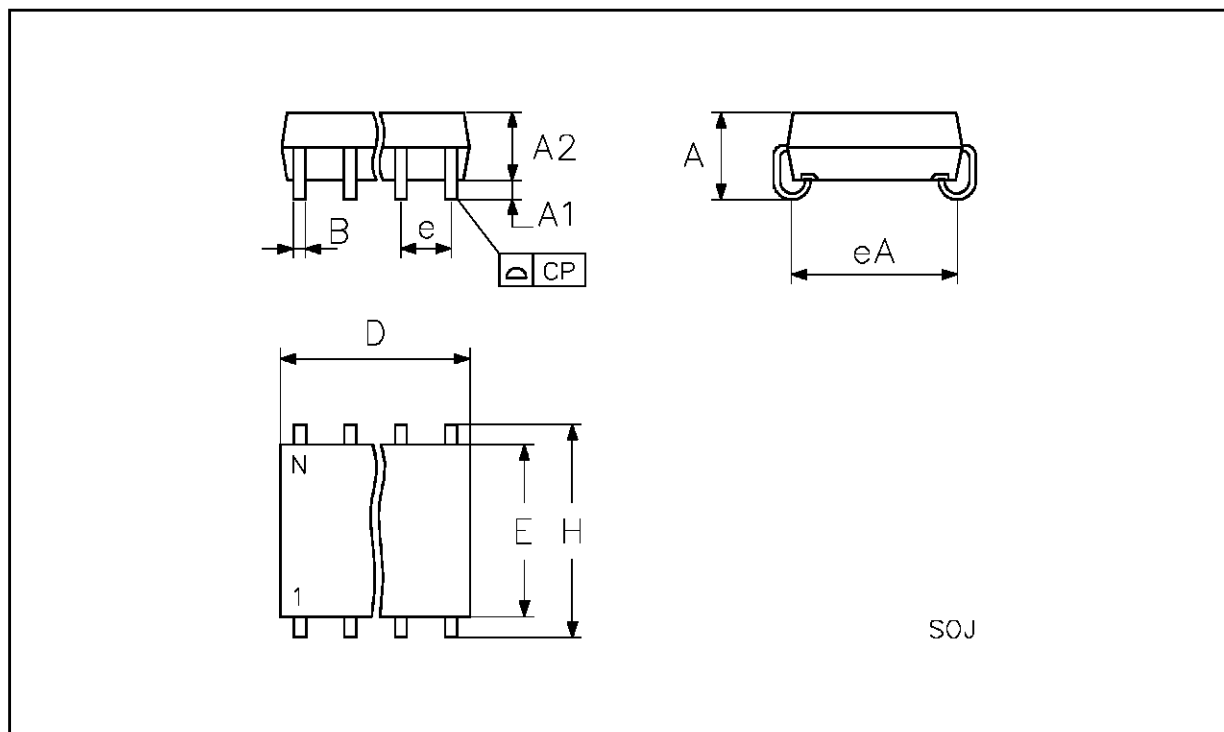
PSDIP-α

Drawing is out of scale

SOJ28 - 28 lead Plastic Small Outline J-lead, 300 mils

| Symb | mm | | | inches | | |
|------|------|-------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | 3.05 | 3.56 | | 0.120 | 0.140 |
| A1 | | 0.71 | 0.91 | | 0.028 | 0.036 |
| A2 | | 2.29 | 2.39 | | 0.090 | 0.094 |
| B | | 0.36 | 0.48 | | 0.014 | 0.019 |
| D | | 17.81 | 18.06 | | 0.701 | 0.711 |
| E | | 7.42 | 7.59 | | 0.292 | 0.299 |
| e | 1.27 | – | – | 0.050 | – | – |
| eA | | 6.65 | 6.91 | | 0.262 | 0.272 |
| H | | 8.51 | 8.81 | | 0.335 | 0.347 |
| N | | 28 | | | 28 | |
| CP | | | 0.10 | | | 0.004 |

SOJ28



Drawing is out of scale

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